COMMUNICATING INSTRUCTION RESULTS IN PROCESSORS
AND COMPILING METHODS FOR PROCESSORS

[ABSTRACT OF THE DISCLOSURE]

A processor, such as a VLIW processor capable of
software-pipeline execution, includes an instruction
issuing unit 10 for issuing, in a predetermined
sequence, instructions to be executed. The sequence of
instructions includes preselected value-producing
instructions which, when executed, produce respective
values. Instruction executing units 14, 16, 18 execute
the issued instructions. A register file 20 has a set
of registers, for storing values produced by the
executed instructions. In operation the processor
assigns the values produced by the value-producing
instructions respective sequence numbers according to
the order of issuance of their respective value-
producing instructions. Each produced value is
allocated one of the registers, for storing that
produced value, in dependence upon the sequence number
assigned to that value. The registers may be renamed
each time a value-producing instruction is issued.

For such a processor the task of the compiler in
register allocation is simplified, and the instruction
set can be more compact.   **[Fig. 1]**